UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,591	07/16/2003	Shih-Hsien Wu	3313-1016P	7448

2292 7590 06/28/2005

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,591	WU ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-18 and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger et al. (6,528,145) in view Nishide et al. (5,827,605) and Zak (6,006,427).

Berger et al. in figure 3 and related text a composite laminate substrate, comprising: at least an inorganic substrate 20 having at least a wiring 26 formed thereon; and

two substrates, comprising print circuit boards (column 10, lines 32-45 and column 12, lines 44-46) located on two sides of said inorganic substrate, having circuits for electrical connections between outer input/output ports and said wiring of said inorganic substrate through said print circuit boards (substrates).

Berger et al. do not teach the print circuit boards being organic print circuit boards and at least a passive component formed in/on the inorganic substrate.

Nishide et al. teach in figure 1 and related text an inorganic substrate 1, 2 having at least a passive component 4, 5, 8 selected from a group consisting of capacitor, inductor and resistor, formed therein/thereon, and circuits for electrical connections

between outer input/output ports and said passive component of said inorganic substrate.

Zak teaches print circuit boards being organic print circuit boards, and the advantages of using organic print circuit boards (column 2, lines 40-45).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use organic print circuit boards and at least a passive component formed on the inorganic substrate in Berger et al.'s device, such that two organic substrates, located on two sides of said inorganic substrate, having electrical connections between outer input/output ports and said passive component of said inorganic substrate through said organic substrates, in order to reduce the cost of making the device and in order to reduce the size of the device by forming the two organic substrates on both sides of said inorganic substrate and by forming the passive elements within the inorganic substrate, respectively.

Regarding claim 2, prior art teaches the material of said inorganic substrate is selected from the group consisting of ceramic, silicon and glass.

Regarding the process limitations recited in claims 3-4, 7-8, 11, 16-17, 20-21 and 24 ("passive component is made from the process selected from the group consisting of thick film process and thin film process", "passive component is made from a semiconductor fabrication process", "the circuit of the print circuit boards are made separately, and then stacked together to form said organic substrates, " the circuit of the

print circuit boards are made separately, then stack the print circuit boards together, and finally form the circuit of a surface layer with build-up process to form said organic substrates", and "wherein said organic substrate is made on said inorganic substrate with build-up process", .these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 9 and 10, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use at least a passive component on said organic substrate and selected from a group consisting of capacitor, inductor and resistor in prior art's device in order to the device in an application which requires a passive element.

Regarding claim 12, prior art teaches a covering layer, for covering said inorganic substrate, integrating with said organic substrate, and fully embedding said inorganic substrate in said the organic substrate, said covering layer further comprises circuits for providing electrical connections between said passive component and said organic substrate.

Regarding claims 13 and 25, Berger et al. teach a bonding layer (BGA) formed between said inorganic substrate and at least one of said organic substrate for bonding the two.

Claims 6 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger et al., Nishide et al. and Zak, as applied to claims 1 and 14 above, and further in view of Czjakowski et al. (6,613,978).

Berger et al., Nishide et al. and Zak teach substantially the entire claimed structure, as applied to claims 1 and 14 above, except each of said organic substrate is composed of a plurality of print circuit boards.

Czjakowski et al. teach a plurality of print circuit boards formed on a ceramic substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form each of said organic substrate of a plurality of print circuit boards, in the device of Berger et al., Nishide et al. and Zak, in order to use the device in an application which requires plurality of print circuit boards.

Response to Arguments

Applicant argues that Berger et al. and the "variant of figure 3" do not teach a PCB located on an inorganic substrate.

Berger et al. clearly state in column 10, lines 32-33 that "The composite substrate is now ready for semiconductor device joining and interconnection to a PCB". Berger et al. further state in column 12, lines 44-46 that "electrical connection can be made to a semiconductor device or a PCB (not shown)". Therefore, Berger et al. teach a PCB located on an inorganic substrate.

Applicant argues that Berger et al. use a BGA to join the substrate to the PCB, and the bonding layer of the present invention is quite different from the BGA.

Although the bonding layer of the present invention is quite different from the BGA, Berger et al. still use a BGA to bond the substrate to the PCB, and still teach a PCB located on an inorganic substrate, as claimed.

Applicant argues that an artisan would not be motivated to combine the references, because the examiner's suggestion to reduce the cost of making the device would not motivate one skilled in the art to think about using a combination of inorganic and organic substrates and the use of a plurality of organic circuit boards on each side of the inorganic substrate.

The examiner does not suggest that one skilled in the art would think about using combination of inorganic and organic substrates and using plurality of organic circuit

boards on each side of the inorganic substrate in order to reduce the cost of making the device. Berger et al. teach combination of inorganic and PCB substrates and using plurality of circuit boards (PCB's) on each side of the inorganic substrate. Berger et al. do not teach a PCB being an organic PCB. One skilled in the art would be motivated to combine the references in order to use an organic PCB in Berger et al.'s device in order to reduce the cost of making the device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached on 7-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
6/23/05

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800